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March 19, 2003

Via Facsimile 703.872.9318Commissioner for Patents
Washington, D.C. 20231

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TECHNOLOGY CENTER 2800

Re: Serial No.: 09/738,193
Art Unit: 2827
Examiner: David E. Graybill
System, Method and Apparatus for Constructing a Semiconductor Wafer-Interposer Using B-Stage Laminates
Our File: 1384-1023

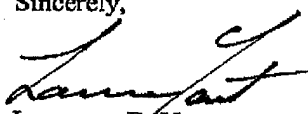
Dear Sir:

Enclosed for filing please find the following items relating (10 pages) to the above-identified application:

- (1) Response Under 37 C.F.R. §1.111 (8 pages);
- (2) Petition Under 37 C.F.R. §1.136 for a Two Month Extension of Time (1 page); and
- (3) Form PTO-2038 authorizing a payment in the amount of \$205.00 (1 page).

If you have any questions or comments concerning this matter, please call the undersigned at your earliest convenience. Otherwise, please accept the enclosed.

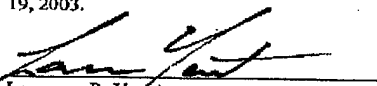
Sincerely,


Lawrence R. Youst
Reg. No. 38,795

Enclosures

Certificate of Transmission Under 37 C.F.R. §1.8

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on March 19, 2003.


Lawrence R. Youst

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Attorney Docket No.: 1384-1023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application: John L. Pierce

Serial No.: 09/738,193

Filed: December 15, 2000

Art Unit: 2827

Examiner: David E. Graybill

For: System, Method and Apparatus for Constructing
a Semiconductor Wafer-Interposer Using B-
Stage Laminates

Commissioner of Patents
Washington, D.C. 20231

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TECHNOLOGY CENTER 2800

Response Under 37 C.F.R. §1.111

Dear Sir:

This is a response to the Office Action dated December 31, 2002, which was due for reply by January 31, 2003. A petition and filing fee for an extension of time for a total period of two months is filed herewith. This response is thereby timely filed on or before March 31, 2003.